REMARKS

Claims 1-4 remain pending in the application. The specification and claims 1 and 2 have been amended without introduction of new matter. Favorable reconsideration is respectfully requested in view of the above amendments and the following remarks.

Before addressing the substantive issues raised in the Office Action, it is noted that in paragraph 20 of the Action, the Office alleges that the Information Disclosure Statement (IDS) filed on 13 December 2004 (and received in the Office on 15 December 2004) fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. On this basis, the Office has merely placed the information in the application file without considering that information.

In response, Applicants respectfully assert that the IDS filed on 13 December 2004 was fully in compliance with the regulations, and that the Office was consequently obliged to consider all of the information disclosed. The basis for Applicants' assertion is 37 C.F.R. §1.98(d), which states:

> (d) A copy of any patent, publication, pending U.S. application or other information, as specified in paragraph (a) of this section, listed in an information disclosure statement is required to be provided, even if the patent, publication, pending U.S. application or other information was previously submitted to, or cited by, the Office in an earlier application, unless:
>
> (1) The earlier application is properly identified in the information disclosure statement and is relied on for an earlier effective filing date under 35 U.S.C. 120; and
>
> (2) The information disclosure statement submitted in the earlier application complies with paragraphs (a) through (c) of this section.

(Emphasis added)

In the present instance, the IDS filed on 13 December 2004 included the following statement on page 1:

> I, the undersigned, hereby state that each item of information listed on the attached PTO/SB-08 of this Information Disclosure Statement was either previously cited by the Office or submitted in copending US. Patent Application No. 09/787,353 naming Richard C. Phelps et al. as inventors and filed June 12, 2001. Because the present application (i.e., U.S. Patent Application No. 10/827,356) relies on US. Patent Application No.

09/787,353 for an earlier effective filing date under 35 U.S.C. § 120, copies of the documents listed on the attached PTO/SB-08 are not being provided herewith; see 37 C.F.R. §1.98(d)(1).

(Emphasis added.)

Because the IDS clearly identified the earlier application upon which the present application relies for an earlier effective filing date under 35 U.S.C. 120, and because the information disclosure statement(s) submitted in the earlier application are understood to comply with paragraphs (a) through (c) of the this section of the regulation, Applicants believe that there was no requirement to submit copies of the cited documents with the IDS of 13 December 2004. Accordingly, it is respectfully requested that the Office consider the information that has, to date, only been put in the file, and that an Examiner-initialed copy of the SB08 forms be returned to Applicant with the next paper to make that consideration of record. For the Examiner's convenience, another copy of the 13 December 2004 IDS is attached herewith.

A number of the drawings were objected to as failing to comply with 37 C.F.R. §1.84(p)(5) because they allegedly include reference signs not mentioned in the description.

With respect to the letter "H" found in Figure 13, the Office's attention is directed to the specification at page 18, lines 21-24 which reads "In step H, a transaction grant message is ... ." As the reference character in question (i.e., "H") is in fact referred to in the specification, no change is believed to be required.

As to the remaining reference characters identified in the Action, Applicants have now corrected the informality by amending the specification to mention the reference characters. No new matter has been introduced.

The drawings were further objected to as failing to comply with 37 C.F.R. §1.84(p)(4) because reference character "A" has been used to designate both "start" in Figure 13 and "assign initial stack positions" on page 17, lines 23-25; because reference character "B" has been used to designate both "assign initial stack positions" in Figure 13 and "receive respective transaction requests" on page 17, lines 30-32; and because reference character "C" has been used to designate both "receive transaction request" in Figure 13 and "determine highest priority level" on page 18, lines 3-7.

In response, Applicants note that when comparison is made with the corresponding description from page 17, line 23 to page 18, line 9, it is evident that the discrepancies that form the bases for these objections have arisen in the description rather than in the drawings.

In particular, step A has been incorrectly identified as "assign initial stack positions" rather than "Start" and this has upset the referencing to subsequent stages B and C, whereas reference to step D has been inadvertently omitted altogether. Thus, instead of amending Figure 13 (which is believed to be correct), Applicants consider it more appropriate to correct the description as follows:

On page 17, line 23, immediately before the first sentence, beginning "The initial set up of the arbitration scheme ...", the following sentence has been added: "The arbitration scheme starts at step A."

On page 17, lines 23-24, the sentence has been amended to read: "The initial set up of the arbitration scheme is to arrange the modules into initial stack positions (step [[A]] B) which are stored in the stack storage means 26."

On page 17, lines 30-32, the sentence has been amended to read as follows: "In step [[B]] C, the arbitration unit 21 receives respective transaction requests from any number of the modules M1 to M5."

And, on page 18, line 9, before the sentence beginning "The control means then masks ..." the following sentence has been inserted: "In step D, the control means obtains the highest priority transaction request."

With these amendments, all reference characters appearing in the figures are also believed to be mentioned in the specification, and the reference characters used in Figure 13 are believed to be compatible with their use in the description. Accordingly, it is respectfully requested that the objections to the figures under 37 C.F.R. §§ 1.84(p)(4)-(5) be withdrawn.

Claims 1-4 were rejected under 35 U.S.C. §112, second paragraph, as allegedly being indefinite. This rejection is respectfully traversed.

First, claim 1 is objected to as being unclear whether it is the address range or the memory map that includes the target address area. In practice, this point is bound up with the Office's second objection as to how the target module can be assigned an address range in the memory map and whether this assignment is the same as the assignment to each module of an address range in the memory map. Reference is made to the description to answer this point.

According to the description on pages 23-24, each module is assigned a respective address region within a predetermined range bounded by specific addresses in the memory map, as illustrated in Figure 26. Each module can address the others simply by using a single address value. Page 24, lines 20-26 explain that the address decoder receives target address data and determines which of the modules (M1 and M2 in this exemplary embodiment) is

assigned the address region into which the target address falls. In other words, the address decoder decides from the target address into which range of addresses the target address falls and thereby identifies the corresponding module covering that range. The output from the address decoder is therefore identification data for the module that contains the requested target address. The answer to the Office's first query is therefore that it is the address range which includes the target address. The wording in claim 1 has been clarified accordingly. In answer to the second query, there is not a second assignment of address range. The wording of claim 1 has therefore been clarified in this respect.

As regards the objection that claim 2 lacks clarity regarding the operation of the control means in relation to the transaction request, reference is made to pages 24 and 25 of the specification together with Figures 25-27. When the target address has been decoded in address decoder 50, Figure 25, the decoded address is supplied to the address/availability comparison means 52 for comparison with information stored in the module availability reception unit 51 to determine whether or not the target module is able to accept the requested transaction. If it is unavailable, the requested transaction is halted. This aspect is covered in claim 1. However, if the module is available, the transaction request is forwarded to the arbitration unit (e.g., unit 21, previously described with reference to Figure 12). Here, the request received in unit 25 is supplied to control means (e.g., the control unit 24) which operates the arbitration scheme. At this point, it should be remembered that only requests for which the target module is available are supplied to the arbitration unit 21 and hence to the request receive means 25. The control means 24 of the arbitration unit 21 is responsible for permitting access to the bus architecture, as described in page 17, line 2 to page 19, line 10. Therefore, when the transaction means of claim 1 determines that a transaction request is in respect of an available target module, it forwards the transaction request to the control means (of the arbitration unit) so that the control means 24 can perform the arbitration process. The wording of claim 2 has been amended in order to clarify this point. The second objection to claim 2, regarding insufficient antecedent basis for the phrase "the transaction request to the control means", has also been addressed by the amendment to claim 2.

In view of the above, claims 1 and 2 are believed to define the claimed subject matter with sufficient particularity and distinctness to satisfy the terms of the statute. Accordingly, it is respectfully requested that the rejection of claims 1-4 under 35 U.S.C. §112, second paragraph, be withdrawn.

Claims 1, 2, and 3 stand rejected under 35 U.S.C. §102(b) as allegedly being anticipated by U.S. Patent Number 4,669,079 to Blum (henceforth, "Blum"). This rejection is respectfully traversed.

In data processors, usually a centralized address decoder decodes all requests directed at it from various parts of the processor, such as individual processing elements (PEs) of an array processor, for example a Single Instruction Multiple Data (SIMD) processor. The problem with such systems is that a single, centralized address decoder cannot handle every request instantly and queues inevitably build up in times of high activity, leading to increased latency for requested transactions. Blum is no exception. Blum describes in column 4, line 53 to column 5, line 36, a centralized bus arbitration system. A single, common arbiter is supplied by each node with the address of another node with which it wishes to communicate. The arbiter assesses the busy state of the addressed node before it grants access.

In contrast, the present invention differs in at least two particular respects. First, each requesting node performs local address decoding of its requesting transaction. Second, that node then masks each transaction for which the target is unavailable.

There are distinct technical and commercial advantages with this approach. One of these is that there is no need to transfer whole address values from the requesting node to the arbiter. Instead, the requesting node generates a decoded target node number, which is then transmitted, thereby saving on interconnect resources. The arbiter has no need to receive actual bus addresses at all. Rather, it only receives requests that have not already been masked out, so that only those requests that can be serviced by the target node are sent from the requesting node.

A second advantage is that each requesting node may perform address decoding according to any local scheme determined by its local conditions or configuration. More flexible system operation is thereby possible since each node can use the address map in different ways. For example, the map shown in Figure 26 may have a different configuration for each requesting unit. Figure 27 illustrates one embodiment of the address decoder, which permits selection of a target node by use of the memory map such that only those transaction requests that are most likely to succeed are actually forwarded for arbitration.

Claim 1 specifies all of the above features. In particular, claim 1 defines "each module comprising:" the reception means as well as the transaction request means, decoding means, comparison means and the transaction means as set out in the remainder of the claim, in order to emphasize the local nature of the process.

In support of the rejection, the Office specifically points to the passage between column 2, line 65 and column3, line 2 of Blum, which states: "there are systems in which the arbiter functions are distributed among various units". Blum states here that the described arrangement may be used in such systems even though it (i.e., Blum's arrangement) is described in the context of a system with a central arbiter. Distributed arbitration is not the issue here and Applicants respectfully contend that the passing reference in Blum is not a specific disclosure that each module contains all of the features specified in claim 1 as now presented.

Thus, Blum does not specifically disclose that each module comprises reception means, transaction request means, decoding means, comparison means and transaction means responsive to the comparison means, all interrelating in the manner claimed. Moreover, in the centralized arbiter system described in Blum, each unit or module informs the arbiter when it is incapable of participating in a transaction because other jobs are being handled, for example. It is not immediately evident that, in the distributed arbiter system postulated in Blum, each unit would compare data about its own availability with identity data locally decoded at the module and relating to a target address. A busy module would be more likely simply to set a flag to inform other modules that it is incapable of accepting a transaction from another module at that time.

Furthermore, the passage in Blum does not suggest, let alone disclose, even in the context of distributed arbitration, the feature of local address decoding where, before a transaction reaches an arbitration stage, a routine is carried out to determine whether or not the target address module is available, as is done in embodiments defined by claim 1. Yet further, the passage relating to distributed arbitration pointed out in Blum misses the point, since the present invention as set out in claim 1 is not a distributed arbitration system at all but provides an effective pre-cursor to arbitration. The local address decoding feature enables a greater degree of certainty for a transaction request sent to an arbiter. Only those transaction requests that are likely to succeed because the target address module is available are actually arbitrated. Blum singularly fails to disclose, teach or suggest such a facility.

Claims 2 and 3 each depend from claim 1, and are therefore patentable over Blum for at least the reasons set forth above.

In view of the foregoing, it is respectfully requested that the rejection of claims 1-3 under 35 U.S.C. §102(b) be withdrawn.

Claim 4 stands rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Blum in view of U.S. Patent Number 5,761,516 to Rostoker et al. This rejection is respectfully traversed.

Claim 4 depends from claim 1, and is therefore patentably distinguishable over the Blum patent for at least the same reasons as set forth above. The Rostoker et al. patent fails to make up for the deficiencies of Blum because it, too, fails to disclose or even suggest the combination of features defined by claim 1. Accordingly, claim 4 is patentably distinguishable over the Blum and Rostoker et al. patents regardless of whether these documents are considered individually or in combination. It is therefore respectfully requested that the rejection of claim 4 under 35 U.S.C. §103(a) be withdrawn.

The application is believed to be in condition for allowance. Prompt notice of same is respectfully requested.

Respectfully submitted,
Potomac Patent Group PLLC

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